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EXAMINER	
PERILLA, JASON M	

ART UNIT	PAPER NUMBER
2611	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/803,047	LIU ET AL.	
	Examiner	Art Unit	
	JASON M. PERILLA	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 July 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,6-10,12,16,18-20 and 23* is/are pending in the application.

4a) Of the above claim(s) *5,15,21 and 22* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5-10,12,15,16 and 18-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-3, 6-10, 12, 16, and 18-20, and 23 are pending in the instant application. Claims 5, 15, 21, 22 are withdrawn.

Response to Amendment/Argument

2. The Applicant's remarks, filed December 22, 2008, have been fully considered.

In view of the Applicant's remarks, the rejections under 35 U.S.C. § 112, second paragraph, have been withdrawn.

The Applicant's remaining arguments rely upon the disqualification of the prior art reference Ito et al (U.S. Pub. No. 2003/0128660). That is, the Applicant has argued against the application of the reference Imamura (U.S. Pat. No. 6862262) alone. The Examiner agrees that the prior art reference Imamura fails to disclose each and every claimed feature of the invention for the reasons set forth by the Applicant; however, the Examiner does not agree that the prior art reference Ito is disqualified as prior art. Therefore, the prior art combination of Imamura in view of Ito is yet applied below.

3. The affidavit filed on December 22, 2008 under 37 CFR 1.131 has been considered but is ineffective to overcome the Ito reference.

To disqualify the prior art reference Ito, the Applicant must show conception of the invention prior to the filing date of Ito (December 31, 2002) and diligence between the conception of the invention and its constructive reduction to practice (i.e. the filing date of this application in the United States; March 18, 2004).

Full conception of the invention is evidenced by the Applicant's affidavit Attachment 1 to be no later than September 26, 2002. Therefore, reasonable diligence must be evidenced between the dates of September 26, 2002, and March 18, 2004.

The following paragraphs from the Manual of Patent Examining Procedure § 2137.06 disclose the pertinent legal standards regarding reasonable diligence:

> An applicant must account for the **entire period** during which diligence is required. *Gould v. Schawlow*, 363 F.2d 908, 919, 150 USPQ 634, 643 (CCPA 1966) (Merely stating that there were no weeks or months that the invention was not worked on is not enough.); *In re Harry*, 333 F.2d 920, 923, 142 USPQ 164, 166 (CCPA 1964) (statement that the subject matter "was diligently reduced to practice" is not a showing but a mere pleading). **A 2-day period lacking activity has been held to be fatal.** *In re Mulder*, 716 F.2d 1542, 1545, 219 USPQ 189, 193 (Fed. Cir. 1983) (37 CFR 1.131 issue); *Fitzgerald v. Arbib*, 268 F.2d 763, 766, 122 USPQ 530, 532 (CCPA 1959) (**Less than 1 month of inactivity during critical period**. Efforts to exploit an invention commercially do not constitute diligence in reducing it to practice. An actual reduction to practice in the case of a design for a three-dimensional article requires that it should be embodied in some structure other than a mere drawing.); *Kendall v. Searles*, 173 F.2d 986, 993, 81 USPQ 363, 369 (CCPA 1949) (Diligence requires that applicants must be specific as to dates and facts.).
>
> **The period during which diligence is required must be accounted for by either affirmative acts or acceptable excuses.** *Rebstock v. Flouret*, 191 USPQ 342, 345 (Bd. Pat. Inter. 1975); *Rieser v. Williams*, 225 F.2d 419, 423, 118 USPQ 96, 100 (CCPA 1958) (Being last to reduce to practice, party cannot prevail unless he has shown that he was first to conceive and that he exercised reasonable diligence during the critical period from just prior to opponent's entry into the field).
>
> The diligence of attorney in preparing and filing patent application inures to the benefit of the inventor. Conception was established at least as early as the date a draft of a patent application was finished by a patent attorney on behalf of the inventor. Conception is less a matter of signature than it is one of disclosure. Attorney does not prepare a patent application on behalf of particular named persons, but on behalf of the true inventive entity. Six days to execute and file

application is acceptable. *Haskell v. Coleburne*, 671 F.2d 1362, 213 USPQ 192, 195 (CCPA 1982). See also *Bey v. Kollonitsch*, 866 F.2d 1024, 231 USPQ 967 (Fed. Cir. 1986) (Reasonable diligence is all that is required of the attorney. Reasonable diligence is established if attorney worked reasonably hard on the application during the continuous critical period. If the attorney has a reasonable backlog of unrelated cases which he takes up in chronological order and carries out expeditiously, that is sufficient. Work on a related case(s) that contributed substantially to the ultimate preparation of an application can be credited as diligence.).

According to the affidavit, the entire delay between the dates of September 26, 2002, and March 18, 2004, is accounted for by the preparation and filing of patent applications in Taiwan and the United States. After the conception of the invention on September 26, 2002, the priority document of the instant application was filed in Taiwan on March 21, 2003 (a six month time period). Between the filing of the priority document in Taiwan and the instant application in the United States, a one year time period elapsed. The great length of time between conception of the invention and the filing of the instant application in the United States has not been accounted for by either affirmative acts of acceptable excuses. The diligence in the preparation of the applications has not been fully evidenced. It was averred in statements 16-18 that three draft specifications for the filing of the instant application in the United States were produced, but the attachments 7-9 are not received by the office. Moreover, translations of any such "email transmittals" should be made into English. Because the entire period during which diligence is required has not been accounted for by either affirmative acts or acceptable excuses, reasonable diligence has not been evidenced by the Applicant.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. § 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-3 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Imamura (U.S. Pat. No. 6862262) in view of Ito et al (U.S. Pub. No. 2003/0128660).

Regarding claim 1, Imamura discloses an apparatus for sampling timing compensation at a receiver of a communication system (abstract; fig. 3), wherein each of at least two pilot signals (fig. 2) comprises a first pilot signal and a second pilot signal (fig. 2; i.e. first and second "CHANNEL ESTIMATION PILOT SYMBOL"), the pilot signals transmitted via respective pilot subchannels (i.e. "each pilot carrier"; col. 6, line 10) and the first and the second pilot subchannels comprising a first and a second pilot indexes (see "A" below) respectively, the apparatus comprising: a pilot subchannel estimator (fig. 3, refs. 103 and 104) for generating frequency responses (fig. 3, ref. 103) of each of the first and second pilot signals (col. 5, line 50) of each pilot signal of each subchannel (col. 5, lines 40-60); a timing offset estimator (fig. 3, ref. 104 illustrated as figs. 4 and 5, ref. 204), coupled to the pilot subchannel estimator (fig. 3, ref. 103), for calculating a timing offset according to a first difference (col. 5, line 48; "differential detection") between the first and second pilots signals of the first subchannel pilot signal, a second difference between the first and second pilot signals of the second subchannel pilot signal ("of each pilot carrier output"; col. 6, line 9) and a "difference" between the first and second differences (col. 6, lines 5-15); and a phase rotator (fig. 4,

ref. 209), coupled to the timing offset estimator, for performing sampling timing compensation according to a phase rotation corresponding to the timing offset. Imamura discloses an apparatus for correcting sampling in an OFDM receiver (fig. 3) which utilizes pilot symbols in each of a plurality of pilot subchannels. Regarding limitation “A” above, as broadly as claimed, each OFDM subchannel of Imamura comprises a separate and distinct “index” or identifier because each is a separate and distinct subchannel. Imamura determines a phase difference between a first and second pilot signals of each of a plurality of pilot subchannel pilot signals in the phase error calculation unit (fig. 4, ref. 204). Imamura further discloses adders (fig. 5, refs. 301 and 302) provided to “add up all differential detection (phase error) outputs of each pilot carrier output” (col. 6, lines 5-10). After summing the phase errors, the accumulated phase error is normalized (fig. 5, refs. 305 and 306; col. 6, lines 18-22) to determine the timing offset using a memory (fig. 4, ref. 206). As broadly as claimed, Imamura discloses that the timing offset is determined, indirectly, according to "a difference between the first and second differences" because the magnitude of the difference between the first and second differences is captured in the normalized output of the phase error calculation unit (fig. 4, ref. 204). Imamura discloses determining "a difference between the first and second differences" of pilot signal frequency responses but does not explicitly disclose "subtracting" a difference between the first and second differences. However, the use of a subtractor to subtract frequency responses among various pilot signals is well known in the art as evidenced by Ito. Ito discloses, in strictly analogous art, a subtractor (fig. 9, ref. 801) which subtracts phase deviations (i.e. a

frequency response) between various pilot signals (¶ 0201) to aide in the determination of an accurate phase deviation result. Therefore, it would have been obvious to one having ordinary skill in the art at the time which the invention was made that the difference determining normalizer of Imamura could be modified to directly determine a subtraction result between differences between pilot signal frequency responses of more than one subchannel because it is a well known and accepted method of determining offsets for reducing sampling timing error which produces only expected and routine results.

Regarding claim 2, Imamura in view of Ito disclose the limitations of claim 1 as applied above. Further, Imamura discloses that the communication system is a multi-carrier "OFDM" system (abstract).

Regarding claim 3, Imamura in view of Ito disclose the limitations of claim 1 as applied above. Further, Imamura discloses that the timing offset estimator further comprises a phase difference calculating device (fig. 5, refs. 301-304) for calculating a phase difference between the first and second frequency responses and a divider (fig. 5, refs. 305 and 306) for calculating the timing offset according to the phase difference and a difference between the first and second pilot indexes (col. 5, line 30 – col. 6, line 40). The pilot indexes are determined according to their position in time. Hence, "the time elapsed between the two data symbols" is associated with the pilot indexes.

6. Claims 6, 10-12, 16, 18, 19, 20, and 23 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Imamura in view of Ito and Singh et al (U.S. Pat. No. 7139320; "Singh").

Regarding claim 6, Imamura in view of Ito disclose the limitations of claim 1 as applied above. Further, Imamura discloses determining a phase difference between the pilot symbols of many subcarriers of a multicarrier system as applied to claim 1 above. (Such difference is indicative of a frequency offset between the transmitter and the receiver.) However, although one skilled in the art is aware that such offset is manifested in the receiver due to poor synchronization of the receiver's local oscillation and sampling frequencies (i.e. Imamura fig. 3, ref. 102; col. 4, lines 10-20) with respect to the operating frequency of the transmitter, Imamura does not explicitly disclose the correction of a sampling frequency offset. However, Singh discloses, in a strictly analogous sampling timing compensation apparatus (fig. 4), compensating both the downconverter frequency (fig. 4, ref. 32) and sampling timing frequency (fig. 4, ref. 34; col. 8, lines 45-55) according to the determined pilot offset (col. 8, lines 15-35). Singh's compensation is performed for frequency synchronization between the OFDM transmitter and receiver (col. 8, lines 52-55). Therefore, it would have been obvious at the time the invention was made that Imamura's (i.e. Imamura in view of Ito) determination of phase offset could be advantageously utilized to update the downconverter and sampling frequencies (Imamura; fig. 3, ref. 102) as taught by Singh because it would achieve frequency synchronization between the OFDM transmitter and receiver. Further, Singh discloses a timing controller (fig. 4, output of 80) for generating a control signal ("FREQUENCY SYNCH ADJUSTMENT") according to the timing offset, wherein the phase of the sampling clock (fig. 4, ref. 82) is adjusted according to the control signal; and an analog-to-digital converter (ADC) (fig. 4, ref. 34) for converting the

symbol according to the sampling clock. These items correspond to the downconverting and sampling (fig. 3, ref. 102) of Imamura (col. 4, lines 10-20).

Regarding claim 10, Imamura in view of Ito and Singh disclose the limitations of the claim as applied to claim 6 above.

Regarding claim 11, Imamura in view of Ito and Singh disclose the limitations of claim 10 as applied above. Further Imamura in view of Singh disclose the remaining limitations of the claim as applied to claim 3 above.

Regarding claim 12, Imamura in view of Ito and Singh disclose the limitations of claim 11 as applied above. Further Imamura in view of Singh disclose the remaining limitations of the claim as applied to claim 3 above.

Regarding claim 16, Imamura in view of Ito and Singh disclose the limitations of claim 10 as applied above. Further Imamura in view of Singh disclose the remaining limitations of the claim as applied to claim 6 above.

Regarding claim 18, Imamura in view of Ito and Singh disclose the limitations of the claim as applied to claim 6 above. Further Imamura in view of Nakahara and Singh disclose a pre-FFT processing device for processing in the time domain (Imamura; fig. 3, ref. 102), a FFT for transforming the symbols to the frequency domain (Imamura; fig. 3, ref. 103), and a, adjusting device for adjusting the operation of the pre-FFT processing device (Singh; fig. 4, refs. 80 and 82).

Regarding claim 19, Imamura in view of Ito and Singh disclose the limitations of claim 18 as applied above. Further, Imamura discloses that the pre-FFT processing device includes an ADC as applied in claim 18 above.

Regarding claim 20, Imamura in view of Ito and Singh disclose the limitations of claim 19 as applied above. Further, Imamura discloses that the pre-FFT processing device further includes a timing controller (fig. 4, output of 80) for generating a control signal ("FREQUENCY SYNCH ADJUSTMENT") according to the timing offset and a clock generator (fig. 4, ref. 82) for controlling the operation of the ADC (fig. 4, ref. 34).

Regarding claim 23, Imamura in view of Ito and Singh disclose the limitations of the claim as applied to claim 6 above.

7. Claims 7, 8, and 17 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Imamura in view of Itoa, Singh, and National ("Application of the ADC1210 CMOS A/D Converter"; National Semiconductor Application Note 245, April 1986 – previously cited).

Regarding claim 7, Imamura in view of Ito and Singh disclose the limitations of claim 6 as applied above. Imamura in view of Ito and Singh do not explicitly disclose that the period of the sampling clock (Tf) is shorter than a sampling interval (Ts) of the ADC. However, it is notoriously known in the art that many modern ADC converters require multiple clock periods to convert an analog signal into a high resolution binary number. Such ADC converters operate in a type of serial fashion to save cost. Specifically, National discloses, on the second column of page 5, that a 500kHz clock could be utilized by the disclosed ADC to create a 12 bit digital representation of an analog signal in 26us. That is, the period of the sampling clock (a 500kHz clock has a 2us period) is more frequent (shorter) than the sampling output interval (every 26us). Therefore, it would have been obvious to one having ordinary skill in the art at the time

which the invention was made to utilize a serial fashion output ADC converter as disclosed by National having a longer sampling interval than sampling clock interval in the apparatus of Imamura in view of Nakahara and Singh because it would save cost.

Regarding claim 8, Imamura in view of Ito, Singh, and National disclose the limitations of claim 7 as applied above. Further, Imamura in view of Ito, Singh, and National disclose the remaining limitations of the claim as applied in claim 7 above.

Regarding claim 17, Imamura in view of Ito and Singh disclose the limitations of claim 13 as applied above. Further Imamura in view of Ito, Singh, and National disclose the remaining limitations of the claim as applied to claim 7 above.

8. Claim 9 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Imamura in view of Ito, Singh, and Matheus et al (U.S. Pat. No. 7009932; hereafter "Matheus").

Regarding claim 9, Imamura in view of Ito and Singh disclose the limitations of claim 6 as applied above. Imamura in view of Ito and Singh do not disclose, however, that the clock generator (Singh; fig. 4, ref. 82) comprises a PLL. Rather, Singh illustrates and discloses a Numerically Controlled Oscillator (NCO). However, the use of phase locked loop circuits as oscillators is notoriously known in the art as taught and disclosed by Matheus (fig. 5, ref. "CORR1"; col. 15, lines 10-12). Therefore, it would have been obvious to one having ordinary skill in the art at the time that the invention was made to utilize a PLL in place of Singh's NCO to generate a clock signal because the use of a PLL is well known and accepted in the art.

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to JASON M. PERILLA whose telephone number is (571)272-3055. The examiner can normally be reached on M-F 8-5 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh M. Fan can be reached on (571) 272-3042. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Jason M Perilla/
Primary Examiner, Art Unit 2611
February 19, 2009

/jmp/